Implementation of Upper Voltage Control Circuit in Static NOR Gate & Domino NOR gate using Microwind

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Abstract- Upper Adaptive voltage level circuit (UAVL) – with its control signal, can supply more dc voltage to the load in active mode & reduced voltage in standby mode is developed. This circuit reduces the power dissipation in electronics. The reduction in power dissipation decreases the leakage current. This circuit is implemented in DSCH & Microwind for 90 nm . The power consumption of upper adaptive voltage level circuit of Domino nor gate is 18% less than domino nor gate. The power dissipation of it is 18 % less than domino nor gate

Index Terms - Upper Adaptive Voltage Level circuit (UAVL), Subthreshold leakage, Domino NOR, Domino NOR with AVL

1. INTRODUCTION

Domino style incorporates clk inputs to all gates.The operation of these gates is divided into 2 phases. The phases are precharge & evaluation . In the precharge phase gate outputs are charged to high level voltage because PMOS transistors are controlled by clock input which in this phase is low .In the evaluate phase, the outputs of the gate can conditionally change to low voltage level. The logic of the gate is implemented only with NMOS transistors those transistors dictate if the outputs will be connected to the low voltage level to be discharged or not.

2. RELATED WORK

2.1 Static NOR gate

Depending on the inputs pmos & nmos is switched on or off. For example data1 & data2 are 01 respectively pmos2-3 is on , nmos1-1 is off & pmos1-2 is off & nmos2-4 is on .So there is no path for output to charged to Vdd & consequently output is low.

2.2 Domino NOR gate

Domino circuit works in 2 phase, during precharge state i.e when clkdomino is low pmos is charged so that output is high driven to Vdd, during evaluate phase i.e clkdomino is high nmos is turned on for example when 01 is given to data1 & data2 respectively nmos1_3 is in off state & nmos2_2 is turned on so output is pulled down to 0 volt through nmos switches.This logic works in evaluate phase

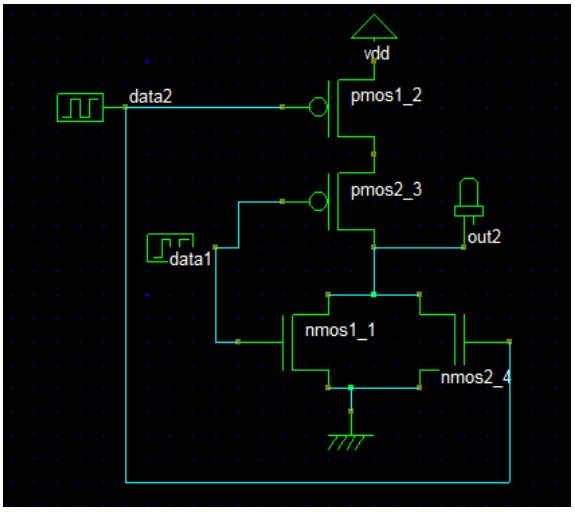

Figure1. Static NOR gate

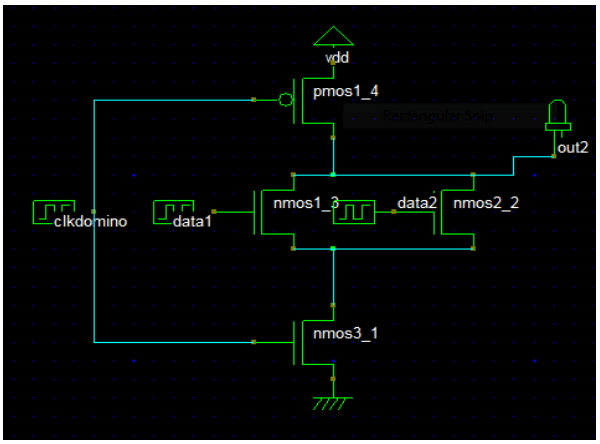

Figure 2. Domino NOR gate

3. PROPOSED WORK

3.1.UPPER ADAPTIVE VOLTAGE LEVEL CIRCUIT (UAVL)

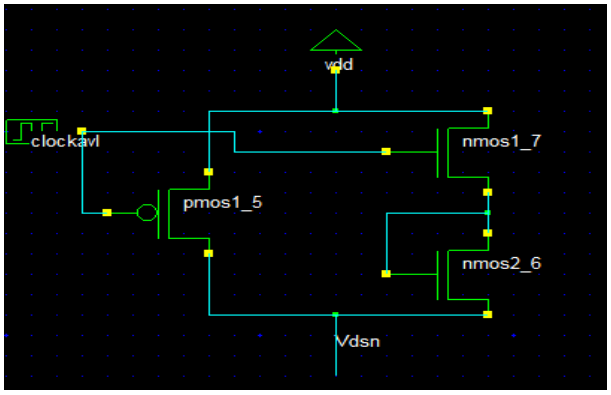

Figure 3. Upper Adaptive Voltage level circuit (UAVL)

An UAVL circuit, in general, consists of a single PMOS switch and m weakly connected Nmos switches connected in series . Here m=2 is considered. When load circuit is in active mode ,pmos of UAVL supplies Vdd to load & n-SWS is turned off. In standby mode 2 nmos of UAVL is on & supplies reduced voltage i.e Vdsn.

Now, the drain volltage of load is

Vdsn = Vdd – 2v

v is voltage drop in single nmos. Hence, Vdsn is reduced which in turn increases the barrier height of the off-Nmos. Therefore Drain Induced Barrier Lowering (DIBL) effect is reduced and therefore the threshold voltage of the nMOS transistor is increased. This results in a decrease in sub-threshold leakage current of the nMOS transistor in the load circuit.

3.2 Static NOR gate with UAVL

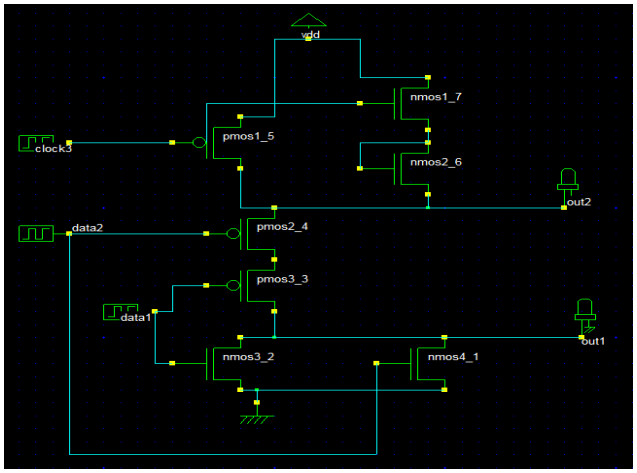

Figure 4. Static NOR gate with UAVL

UAVL supplies Vdd in active mode of load. Depending on inputs to nor gate output follows the logic operation.For example for inputs 01 respectively &clock3 in on condition UAVL supplies Vdd-2v through nmos1-7 & nmos2_6 as data 2is 1 pmos2-4 is off & nmos4-1 is on & data1 is 0 so pmos3-3 is on& nmos3-2 is off ,As there is no path from UAVL to out1 ,output is low.

3.3. Domino NOR gate with UAVL

UAVL supplies Vdd to active load i.e when pmos2-4 is on it is the precharge phase so out1 is driven high.In evaluate phase nmos 5-1 is on & depending on inputs nmos switch remains on or off if on out1 is pulled down through nmos5-1 else it retains the charge.

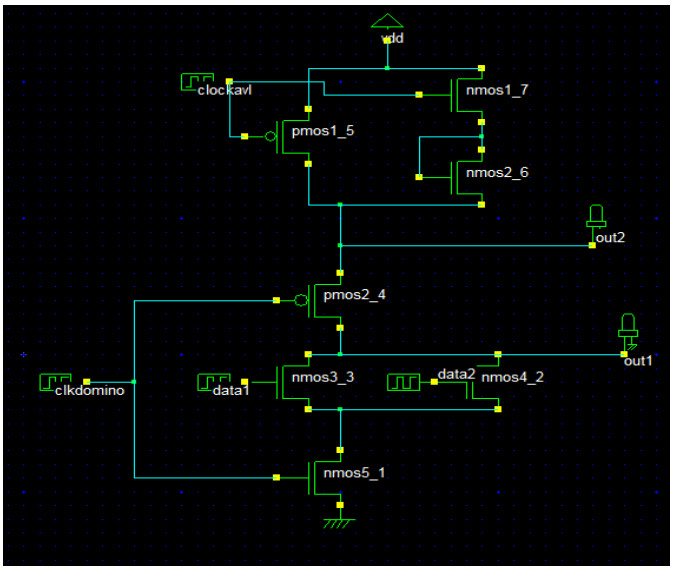

Figure 5. Domino NOR gate with UAVL

4. RESULTS & DISCUSSION

All the simulation results were obtained using Microwind & DSCH tool. The input sequence used is 00 01 10 11 respectively.Any circuit implemented with UAVL has low power consumption & power dissipation.

4.1 Static NOR gate

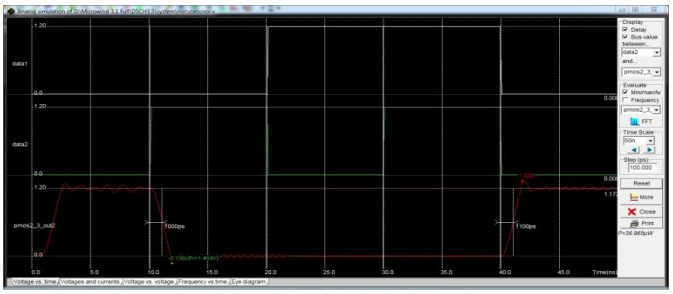

Figure 6. Static NOR gate -voltage curve & power consumption

Static NOR gate has power consumption of 36.965 µW. Power dissipation is 0.037mW. Propagation delay is 1050ps

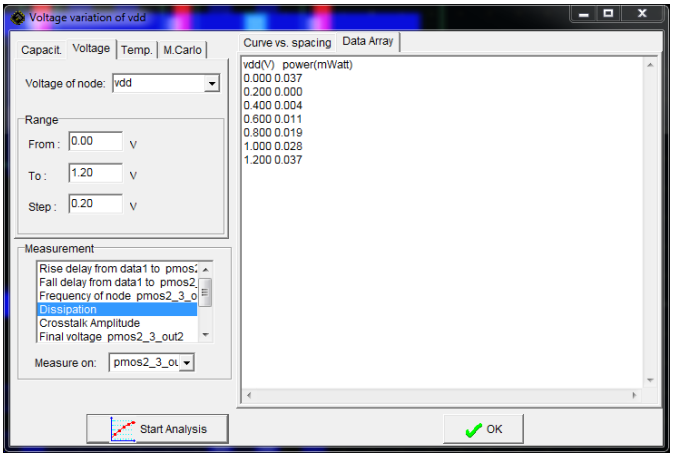

Figure 7. Static NOR gate power dissipation

4.2 Static NOR gate with UAVL

Static NOR gate with UAVL has power consumption of 35.380µW. Power dissipation is 0.035mW. Propagation delay is 950ps

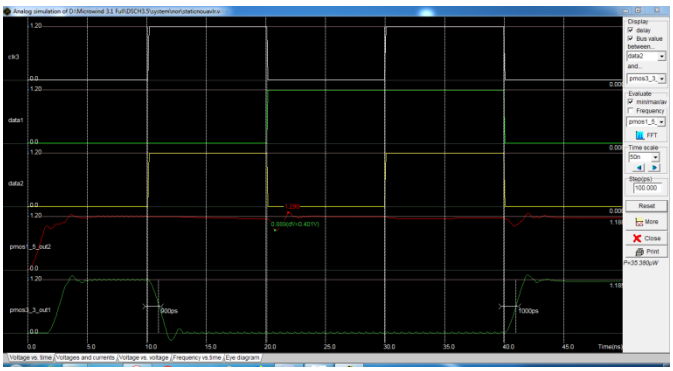

Figure 8. Static NOR gate with UAVL -voltage curve & power consumption

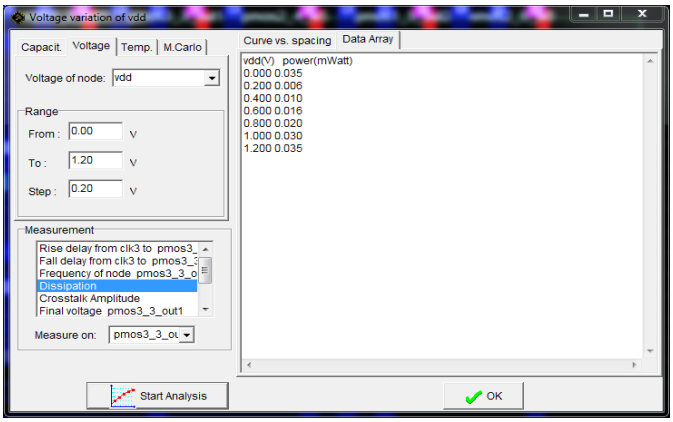

Figure 9. Static NOR gate with UAVL - power dissipation

4.3 Domino NOR gate

Domino NOR gate has power consumption of 59.414µW. Power dissipation is 0.059mW. Propagation delay is 3800ps

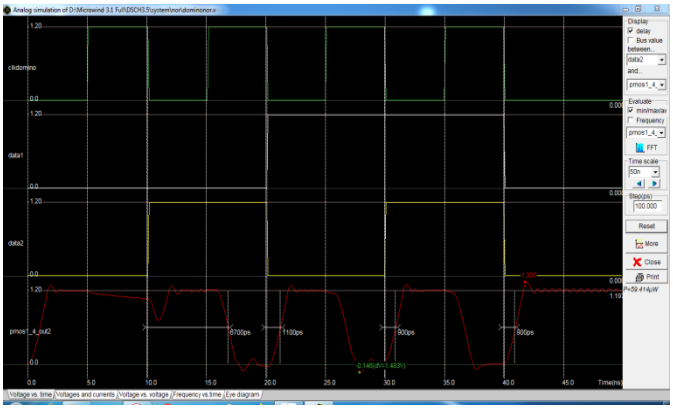

Figure 10. Domino NOR gate -voltage curve & power consumption

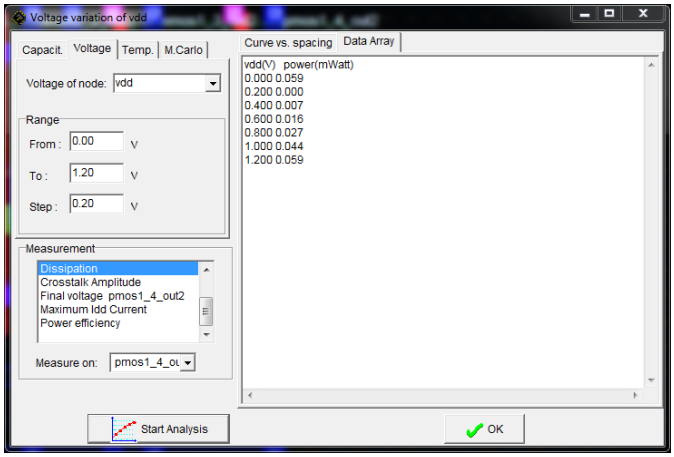

Figure 11. Domino NOR gate power dissipation

4.3 Domino NOR gate with UAVL

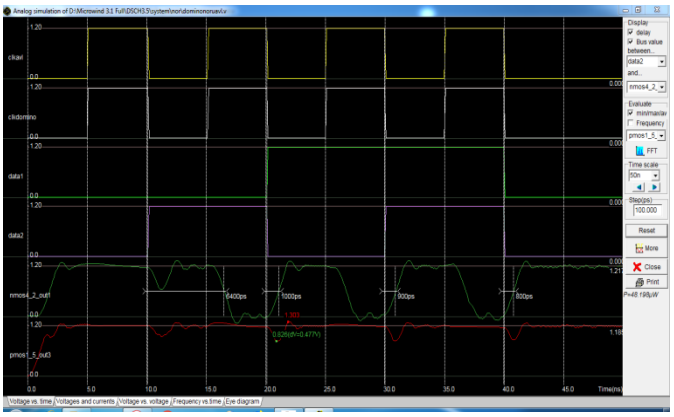

Figure12. Domino NOR gate with UAVL- voltage curve & power consumption

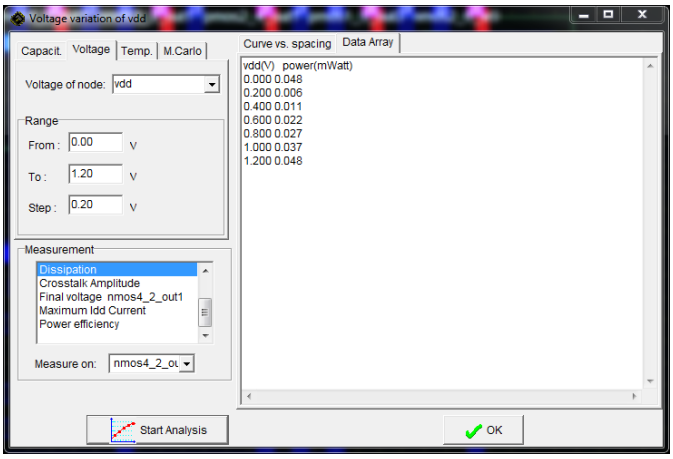

Figure 13. Domino NOR gate with UAVL - power dissipation

Power consumption is 48.198µW . Propagation delay is 3700ps.Power dissipation is 0.048mW .

5. SIMULATION RESULTS

Parameters	Power Consumption (µW)	Power Dissipation (mW)	Idd current at node (mA)	Delay (ps)
Static NOR gate	36.965	0.037	0.376	1050
Static NOR gate with UAVL	35.380	0.035	0.35	950
DOMINO NOR	59.414	0.059	0.395	3800
UAVL with Domino NOR	48.198	0.048	0.393	3700

6. CONCLUSION

Upper Adaptive Voltage Level Circuit which reduces leakage power was developed.This circuit increases the threshold voltage which in connection reduces leakage power .So it can be used in low leakage power applications. It also has reduced power consumption & dissipation..

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